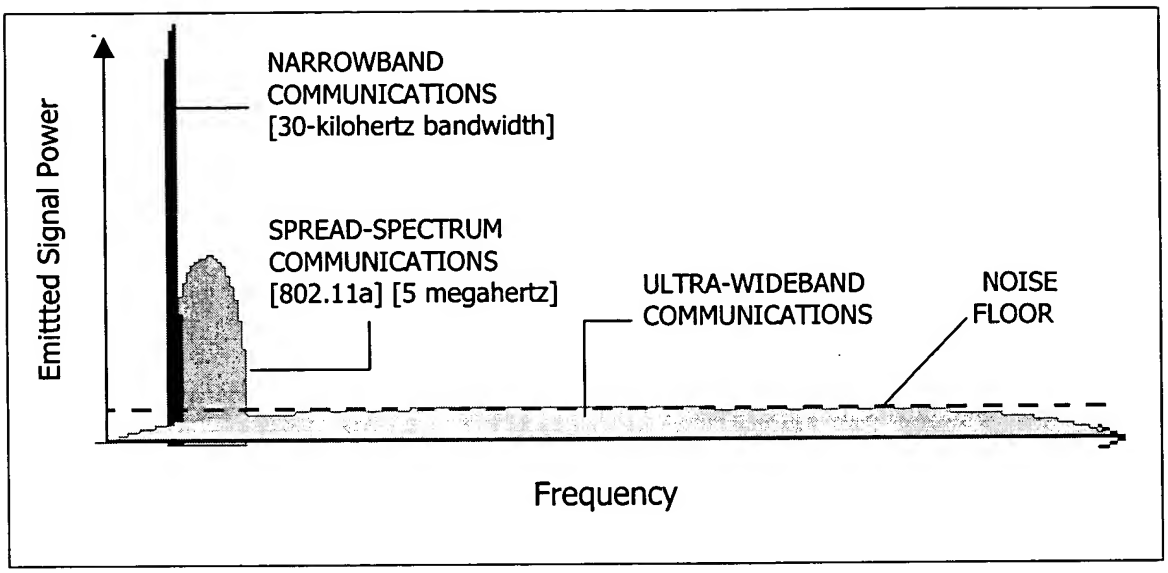


FIGURE 1

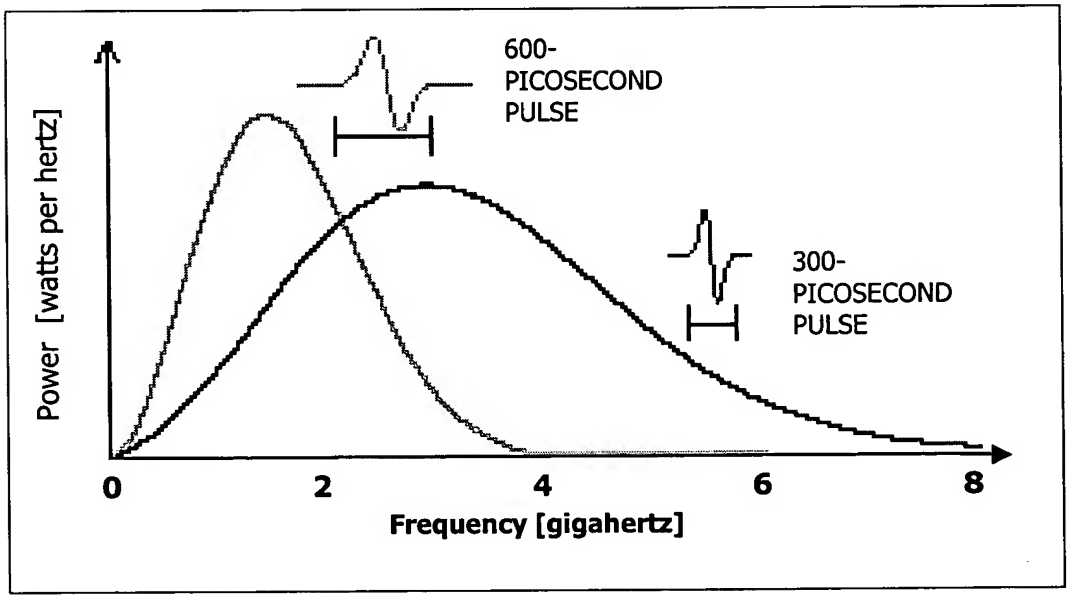


FIGURE 2

FIGURE 3

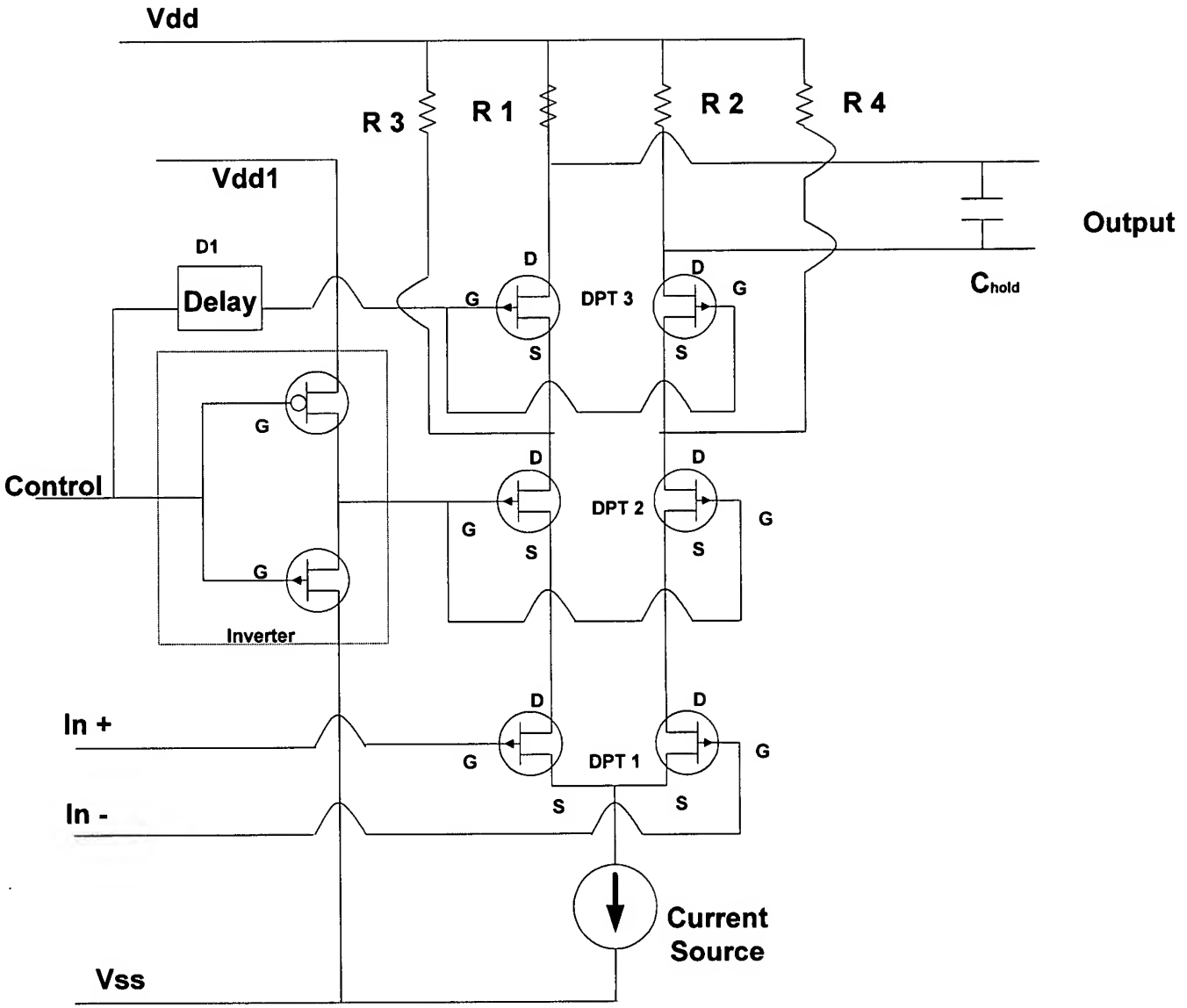

Vdd
R 3
R 1
R 2
R 4
Vdd1
Output
D1
Delay
D
G
S
DPT 3
C_{hold}
Control
G
DPT 2
Inverter
In +
DPT 1
In -
Current Source
Vss

FIGURE 4

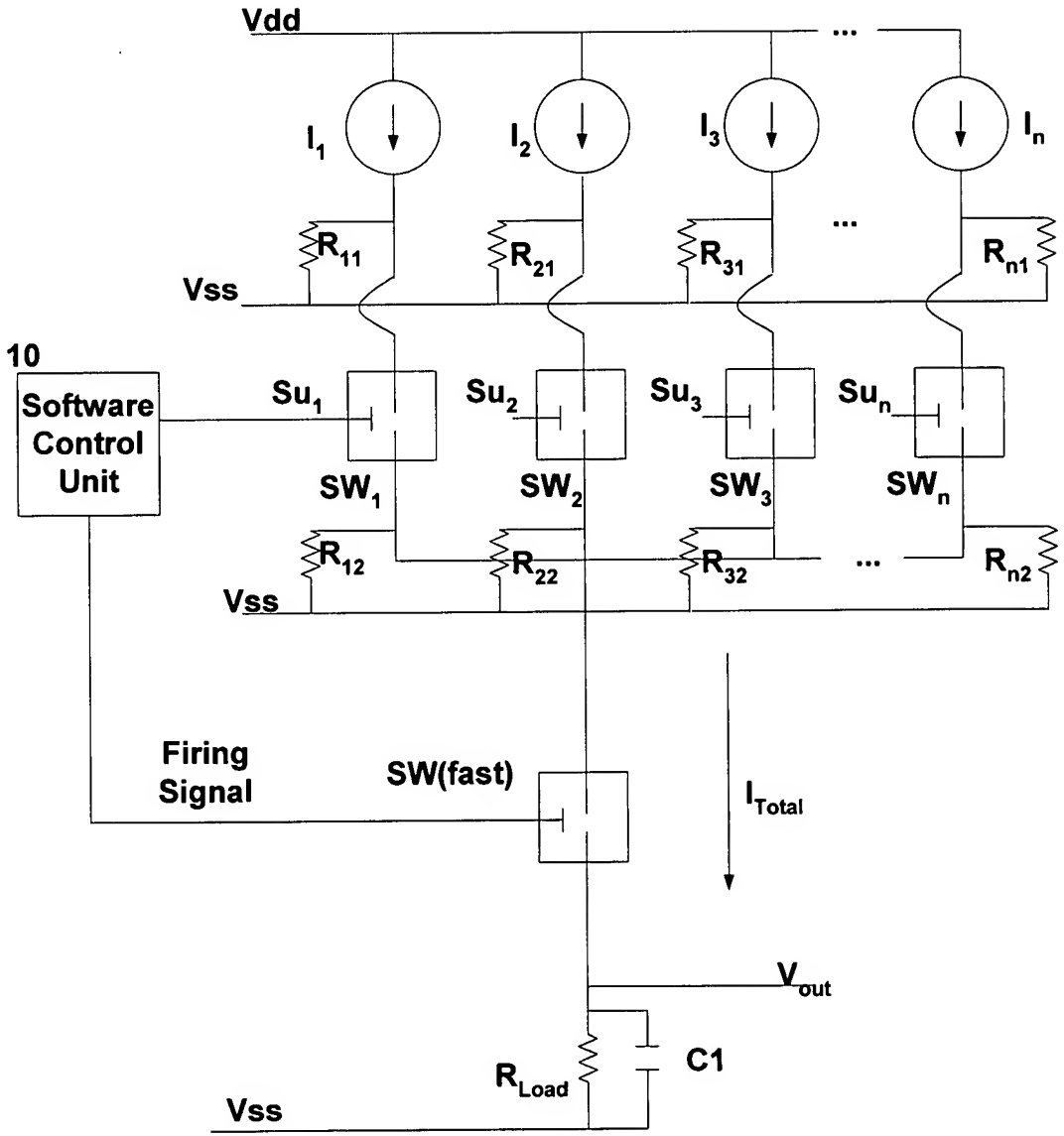

Vdd
...
I_1
I_2
I_3
I_n
R_{11}
R_{21}
R_{31}
R_{n1}
Vss
10
Software Control Unit
Su_1
Su_2
Su_3
Su_n
SW_1
SW_2
SW_3
SW_n
R_{12}
R_{22}
R_{32}
R_{n2}
Vss
Firing Signal
SW(fast)
I_{Total}
V_{out}
R_{Load}
C1
Vss

FIGURE 5

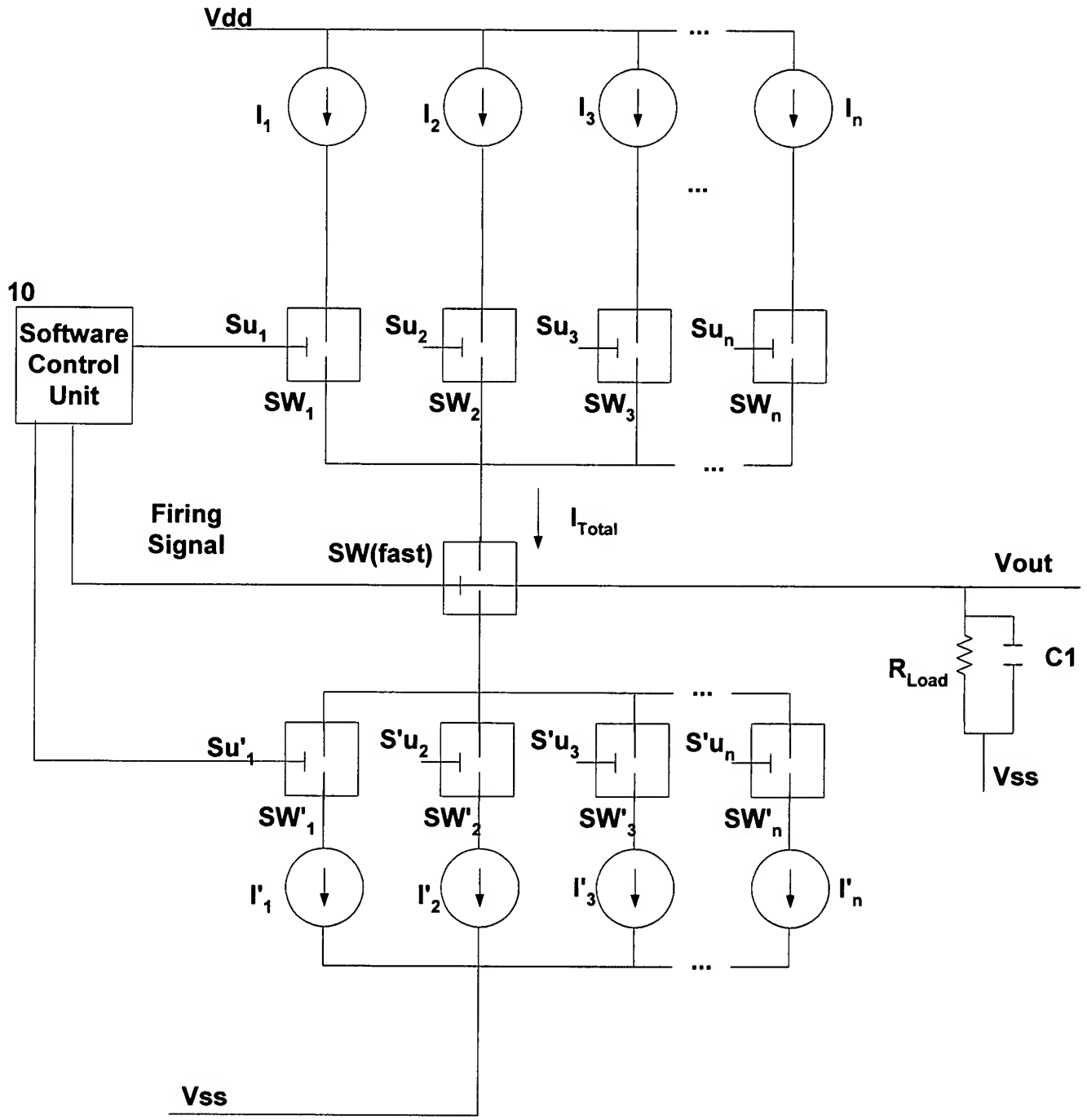
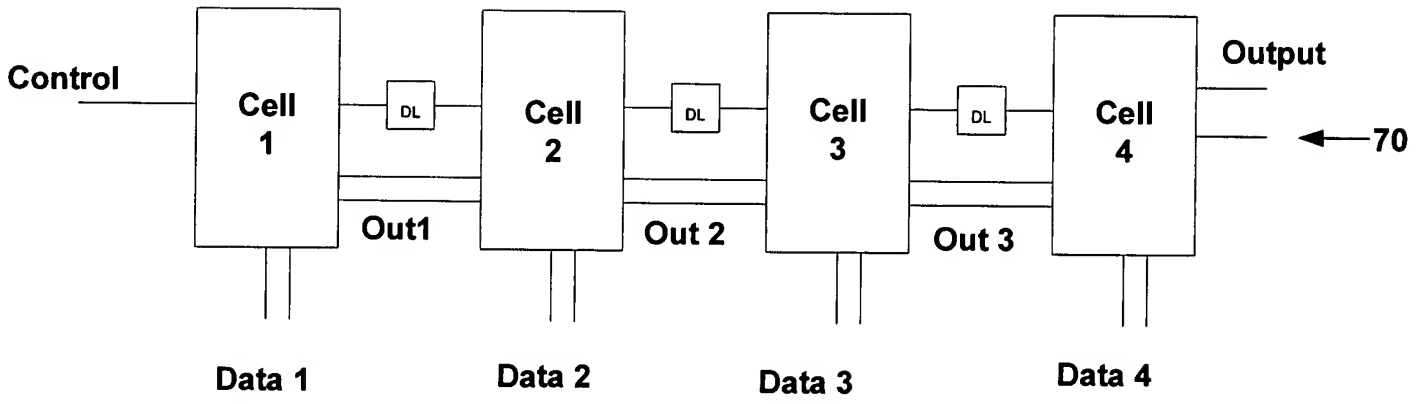

Vdd
I1
I2
I3
In
10
Software Control Unit
Su1
Su2
Su3
Sun
SW1
SW2
SW3
SWn
Firing Signal
ITotal
SW(fast)
Vout
RLoad
C1
Vss
Su'1
S'u2
S'u3
S'un
SW'1
SW'2
SW'3
SW'n
I'1
I'2
I'3
I'n
Vss

FIGURE 6


Control
Cell 1
DL
Cell 2
DL
Cell 3
DL
Cell 4
Output
70
Out1
Out 2
Out 3
Data 1
Data 2
Data 3
Data 4

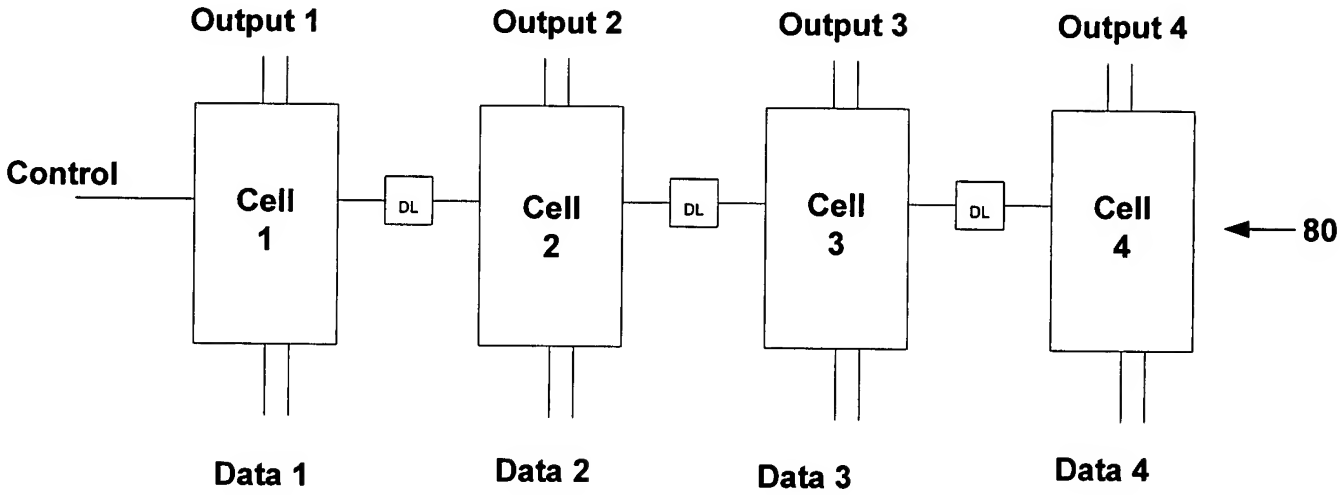

Output 1
Output 2
Output 3
Output 4
Control
Cell 1
DL
Cell 2
DL
Cell 3
DL
Cell 4
80
Data 1
Data 2
Data 3
Data 4

FIGURE 7

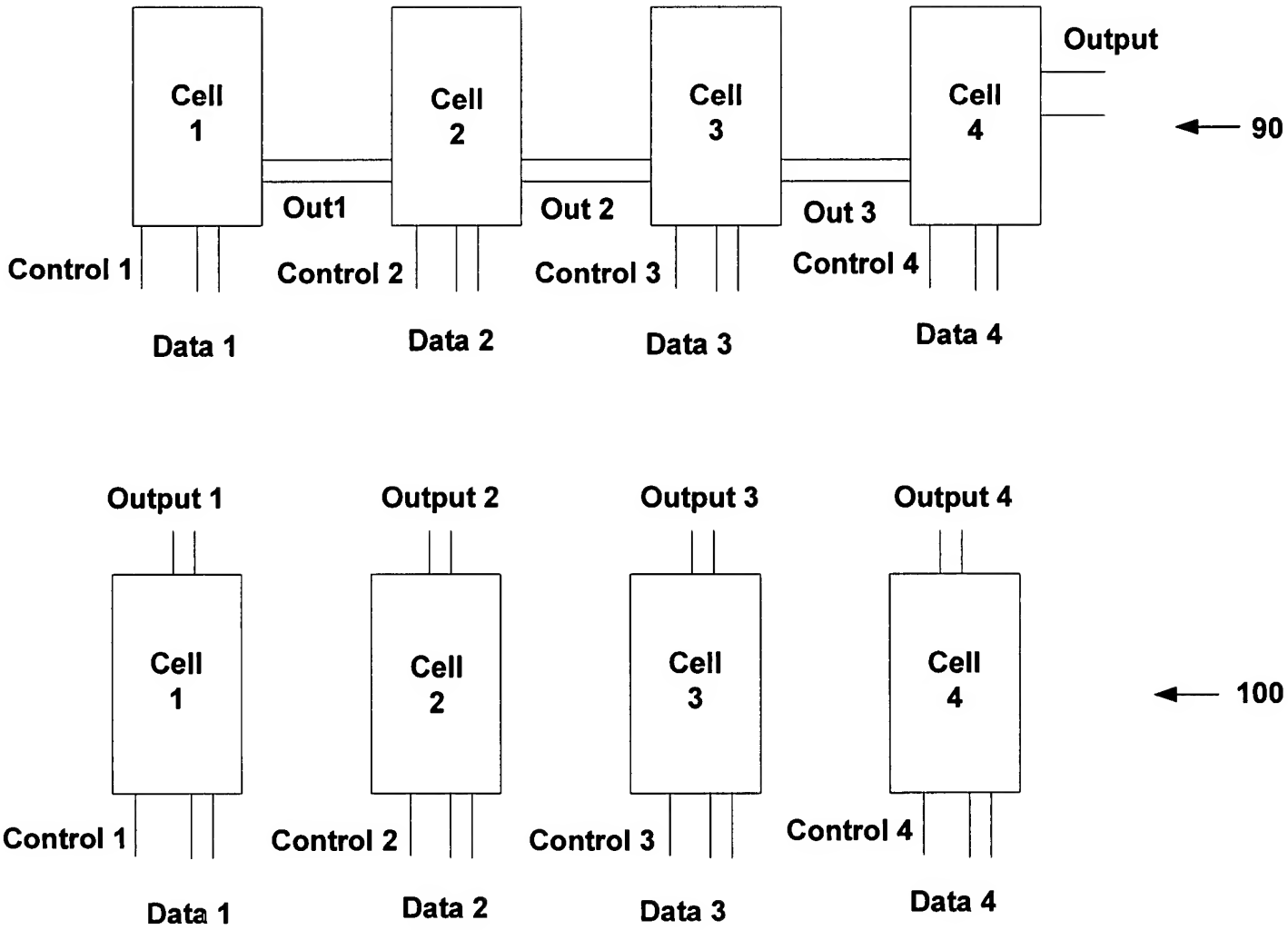

Cell 1
Cell 2
Cell 3
Cell 4
Output
90
Out1
Out 2
Out 3
Control 1
Control 2
Control 3
Control 4
Data 1
Data 2
Data 3
Data 4
Output 1
Output 2
Output 3
Output 4
Cell 1
Cell 2
Cell 3
Cell 4
100
Control 1
Control 2
Control 3
Control 4
Data 1
Data 2
Data 3
Data 4

FIGURE 8

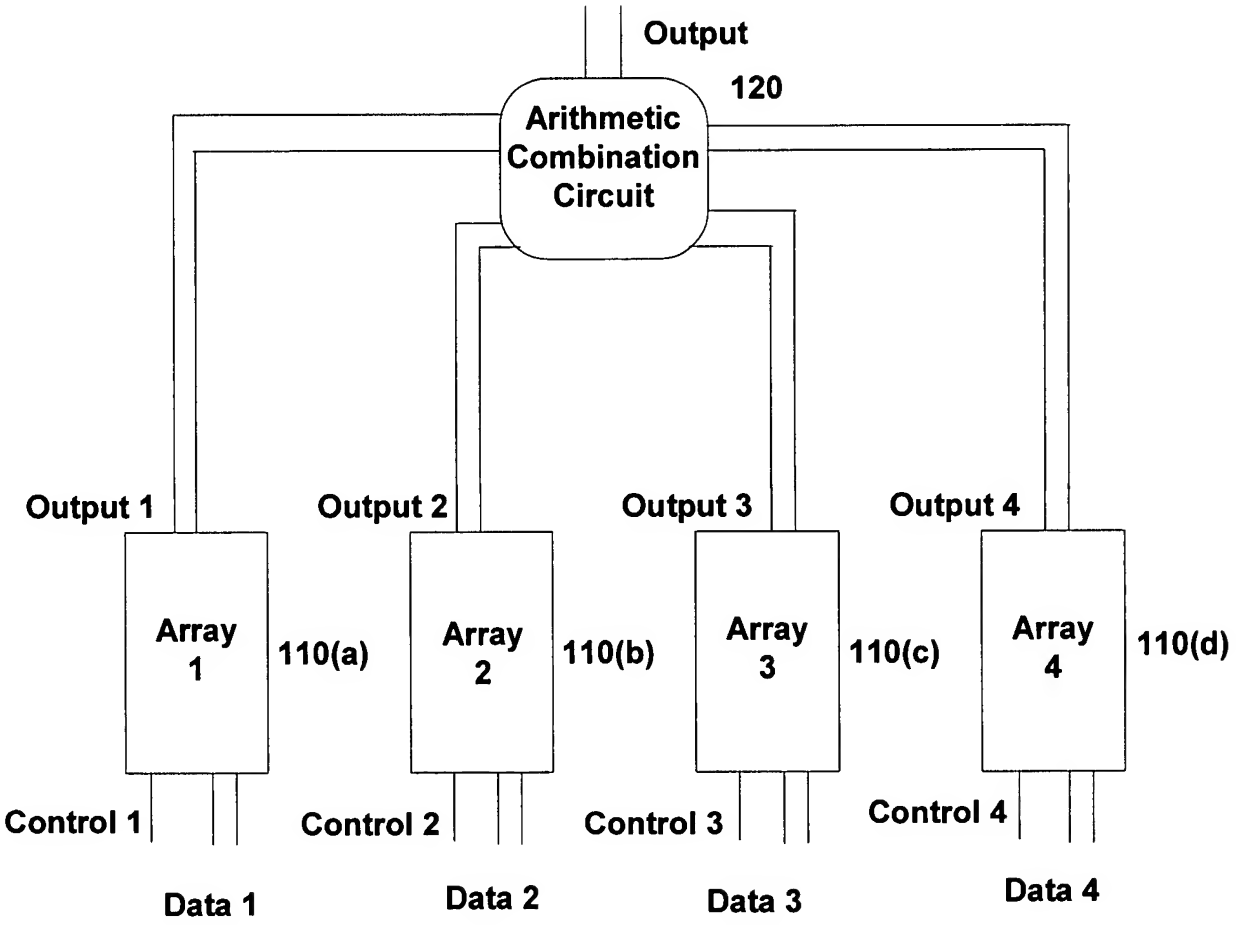

Output
120
Arithmetic Combination Circuit
Output 1
Output 2
Output 3
Output 4
Array 1
110(a)
Array 2
110(b)
Array 3
110(c)
Array 4
110(d)
Control 1
Control 2
Control 3
Control 4
Data 1
Data 2
Data 3
Data 4

FIGURE 9

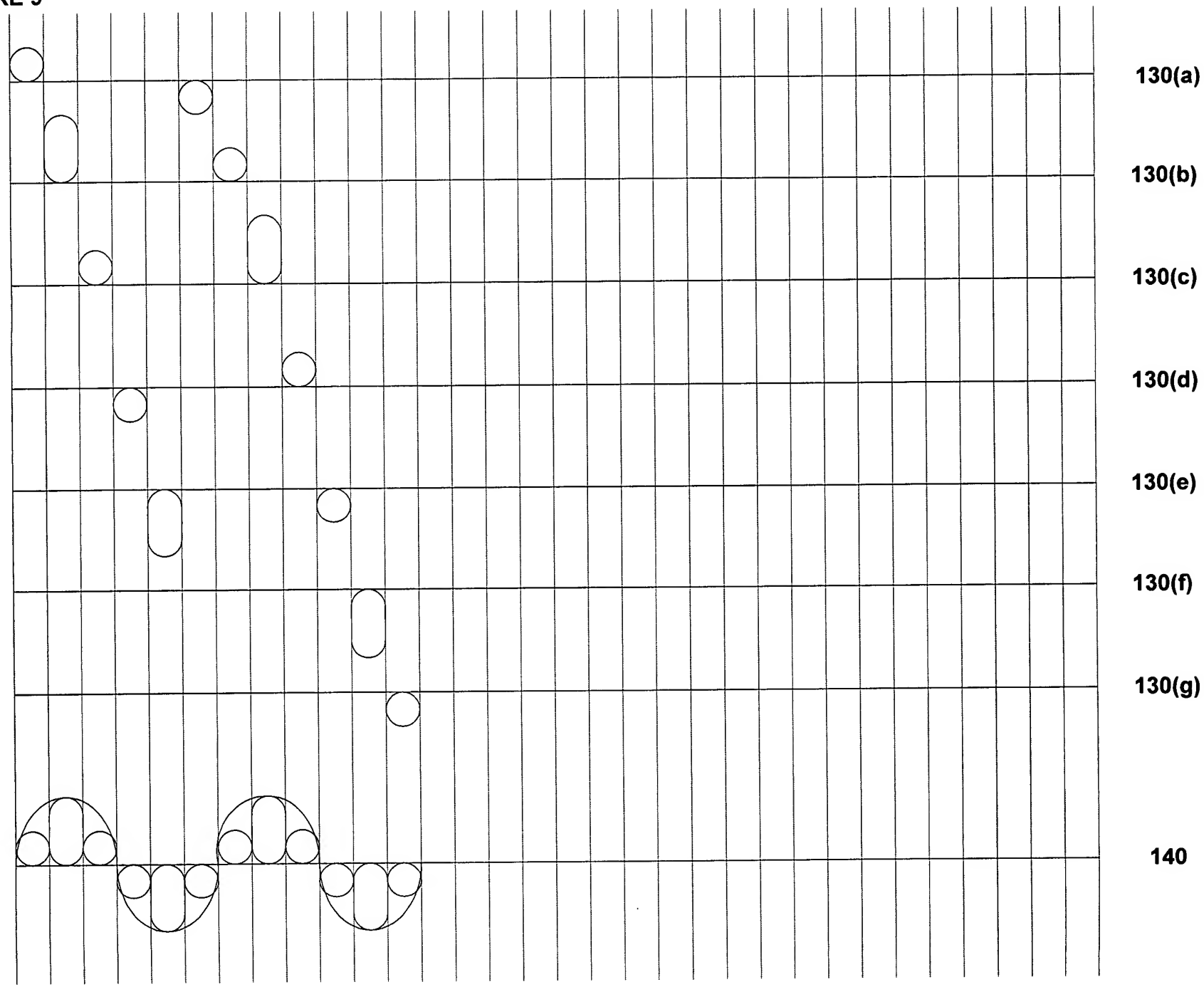
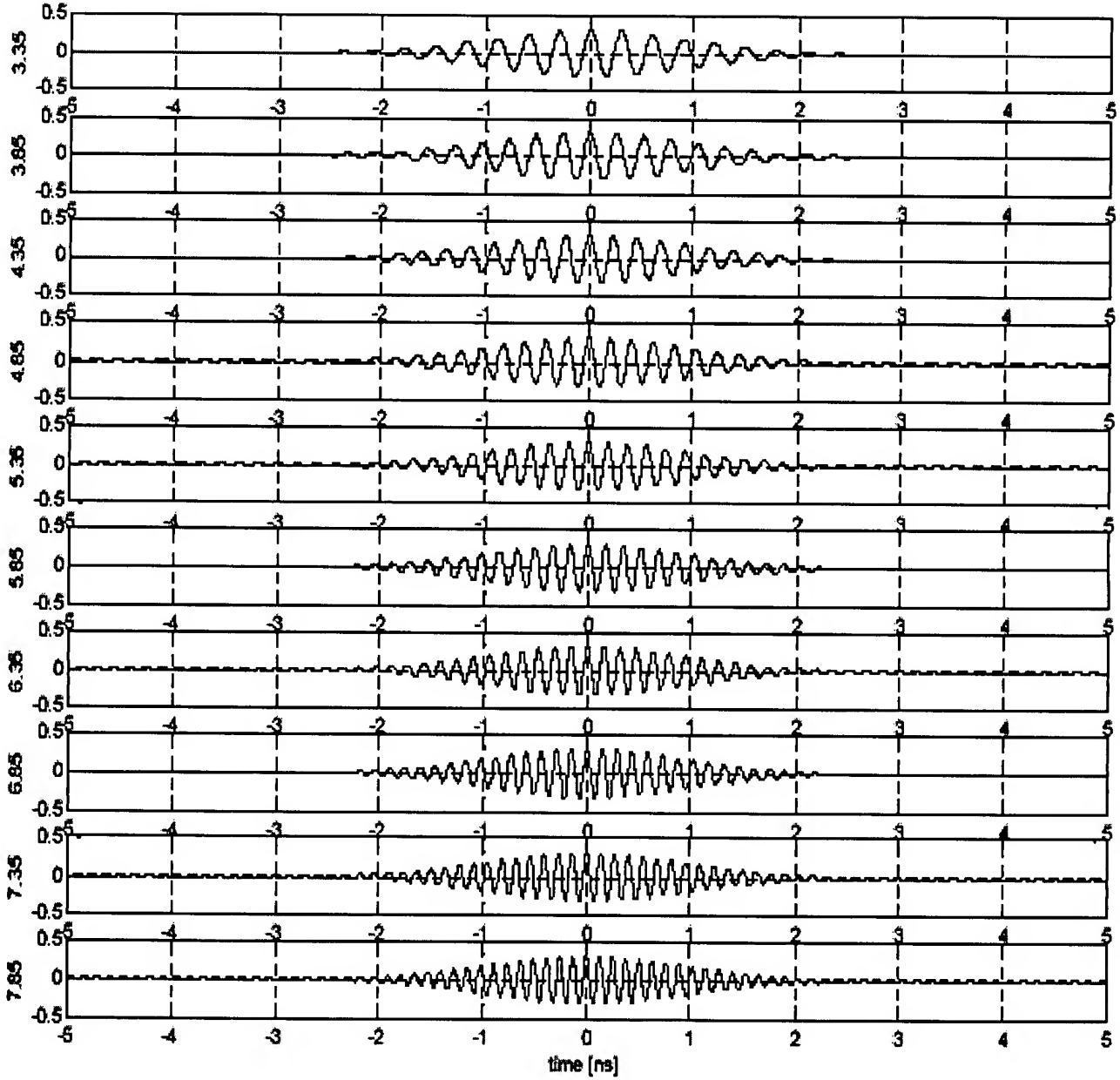


FIGURE 10



150(a)

150(b)

150(c)

150(d)

150(e)

150(f)

150(g)

150(h)

150(i)

150(j)

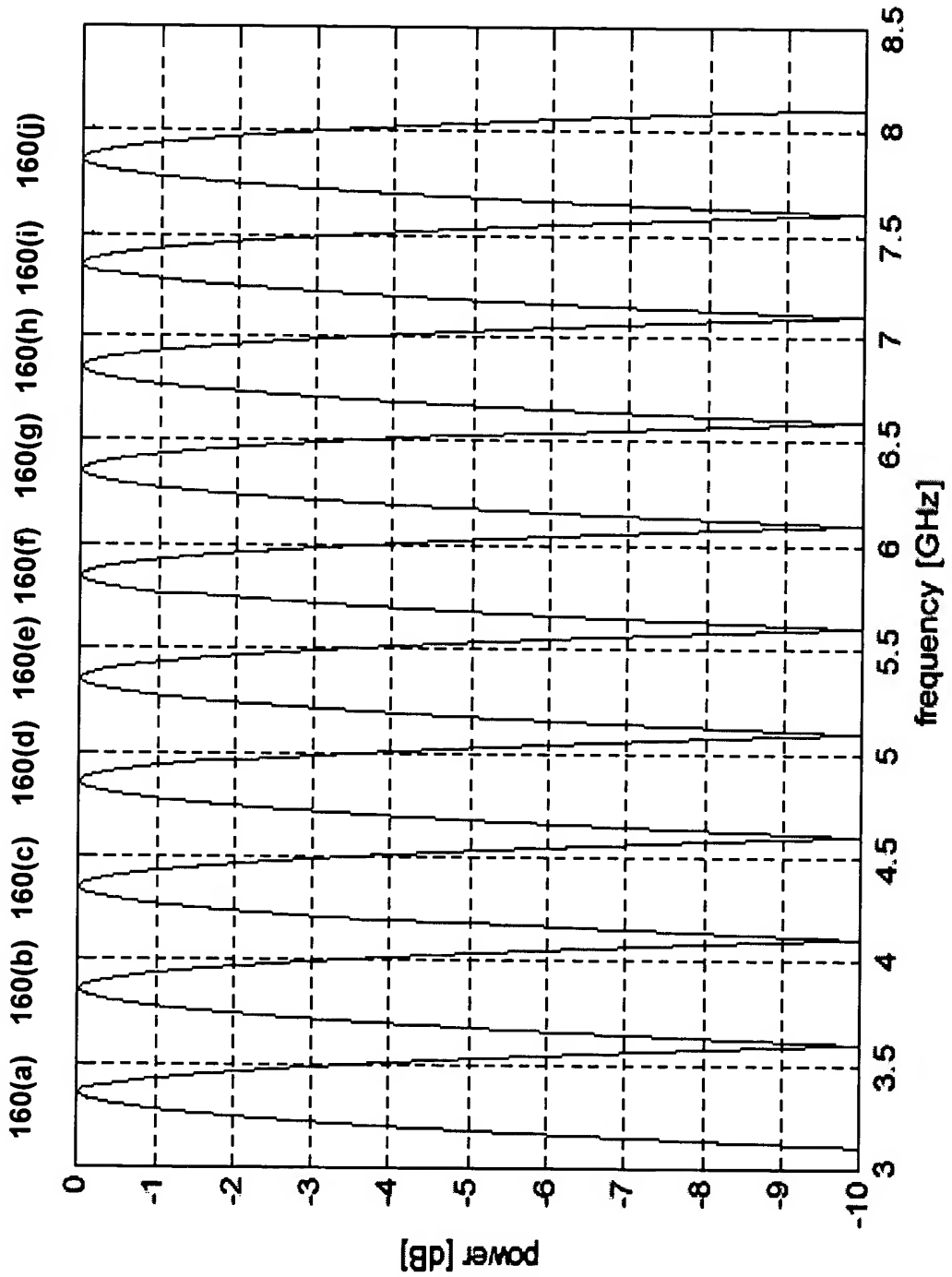

160(a) 160(b) 160(c) 160(d) 160(e) 160(f) 160(g) 160(h) 160(i) 160(j)
power [dB]
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
3
3.5
4
4.5
5
5.5
6
6.5
7
7.5
8
8.5
frequency [GHz]

FIGURE 11

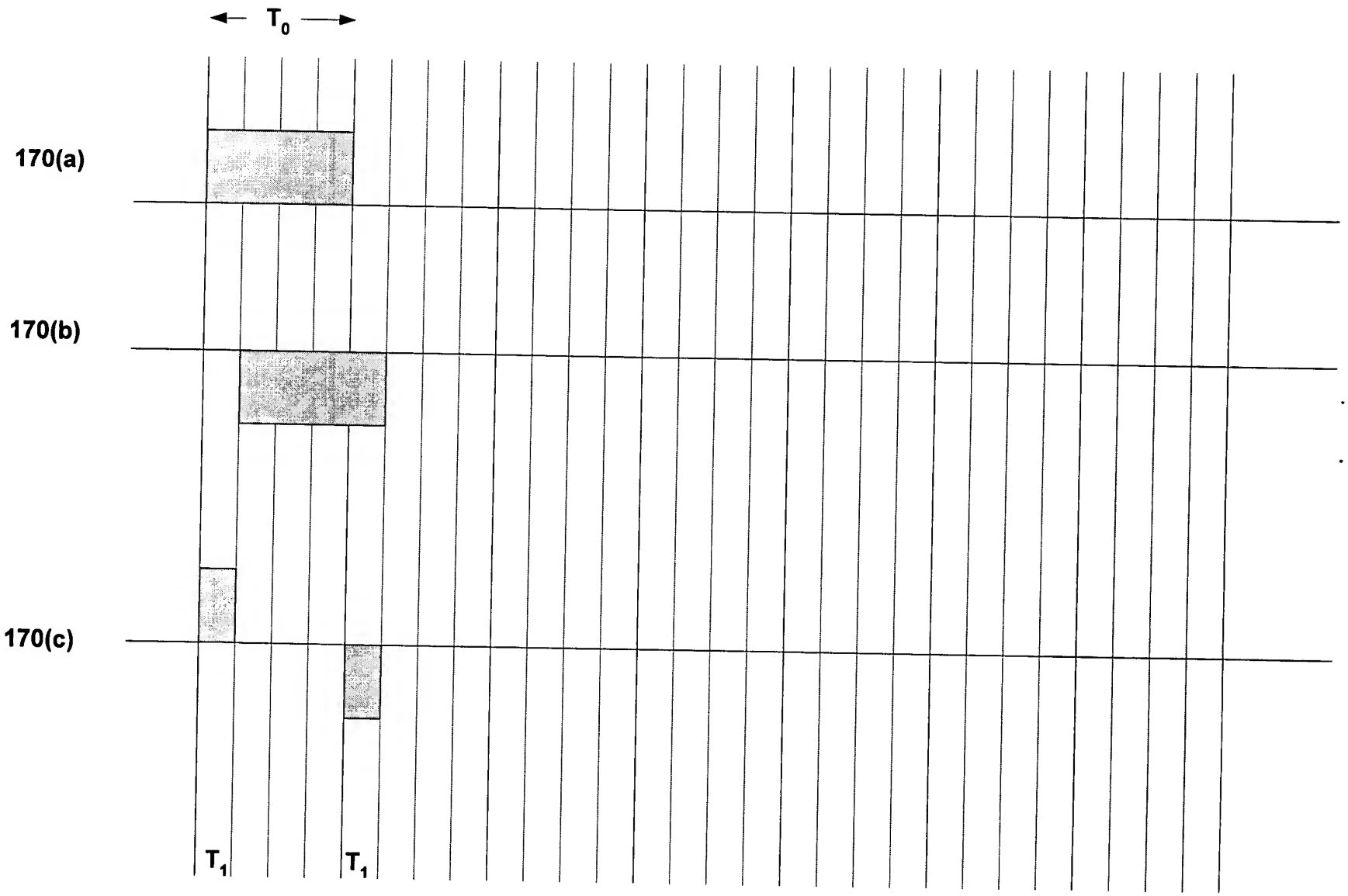



FIGURE 12